# WATWAOS: A Framework for Worst-Case-Aware Tailoring and Whole-System Analysis of Energy-Constrained Real-Time Systems

December 3, 2025
46th IEEE Real-Time Systems Symposium, Boston, MA, USA

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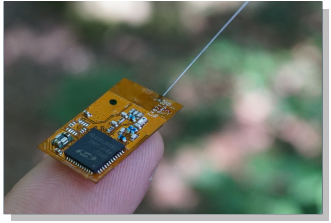
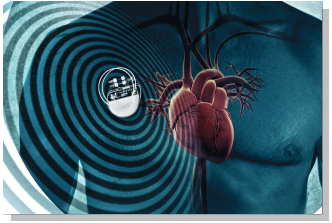
Supported by the DFG under the grant WA 5186/1-1 (Watwa)

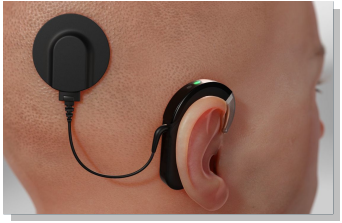
Lehrstuhl für Informatik 4
Systemsoftware

Friedrich-Alexander-Universität
Faculty of Engineering

# Embedded Real-Time Systems

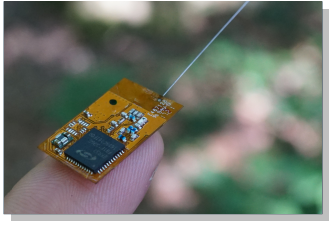


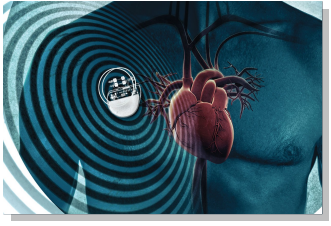


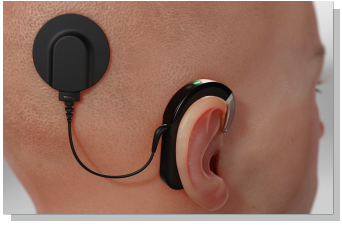


## Requirements

- Safe worst-case timing and energy consumption bounds (WCET/WCEC)
- Energy-efficient operation







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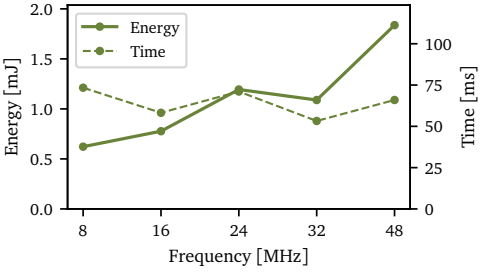
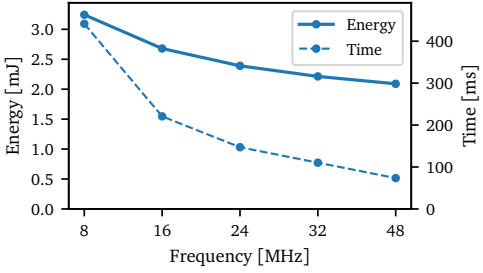
reading sensor data




processing sensor data



# Dynamic Frequency Scaling Approaches

## Dynamic Approaches

- Detect I/O and compute phases and change clock frequency accordingly

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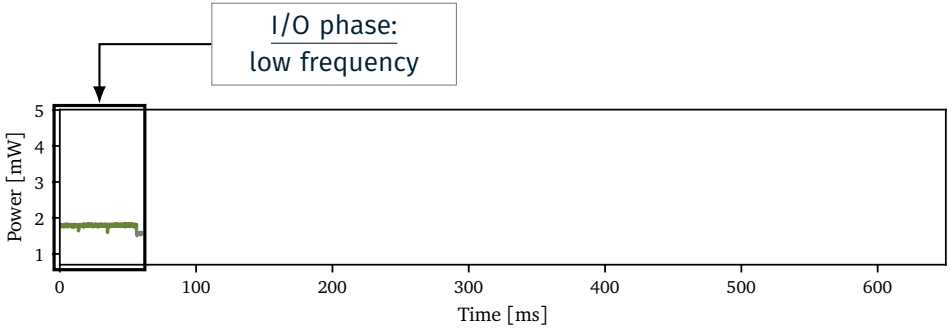

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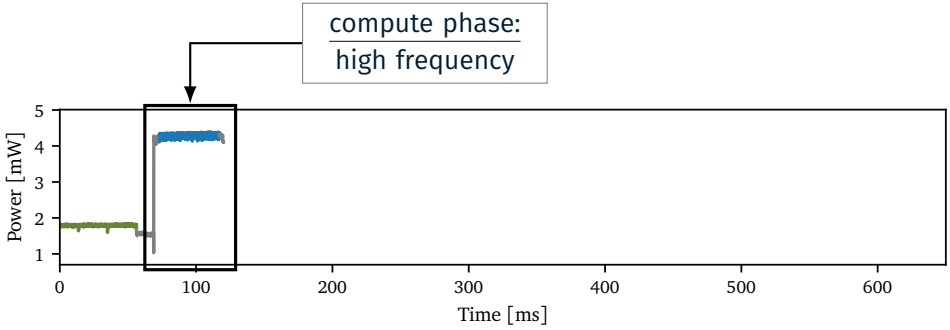

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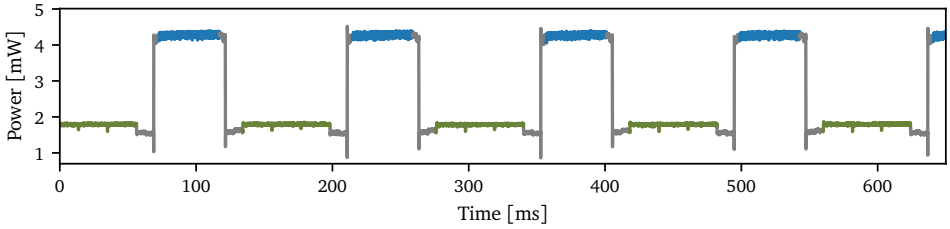

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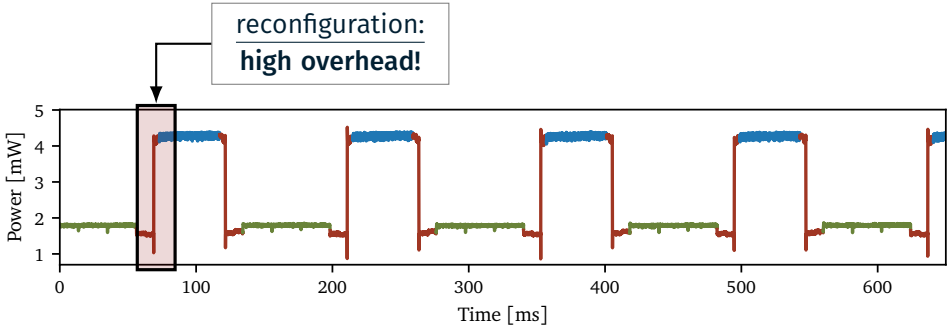
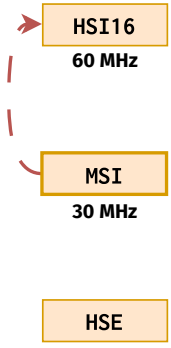


# Clock Trees



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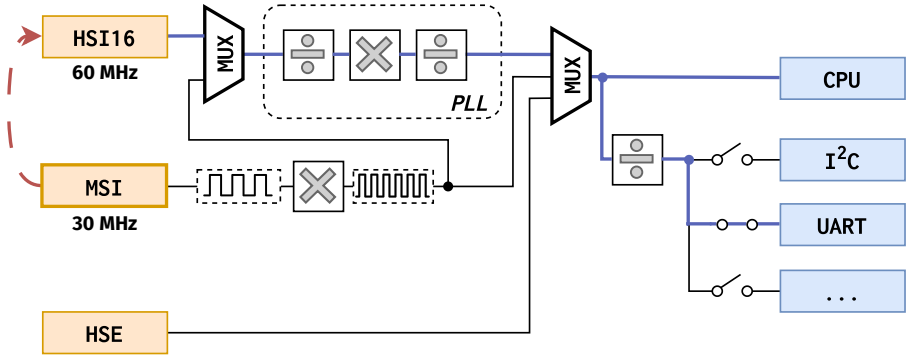

# Problem Statement

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**In a Nutshell:**

- Minimize energy consumption while providing safe WCET/WCEC bounds
  - Construct global Power-State–Transition Graph [ECRTS '18] → perform IPET to get WCET/WCEC
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- Keep analysis and optimization times reasonable
  - Reduce ILP complexity with *node merging* techniques
  - Make use of special solver features

# System Model

## Hardware

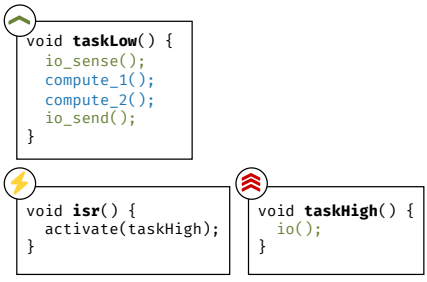
- Resource-constrained system-on-chip platform
- Predictable architecture, no caches
- Complex clock-configuration networks

## Operating System

- Fixed-priority, preemptive scheduler
- Statically known task set
- Independent tasks
- Any number of sporadic task activations ($\rightarrow$ interrupts) allowed

# The WatwaOS Approach (1)

Application:



# The WATWAOS Approach (1)

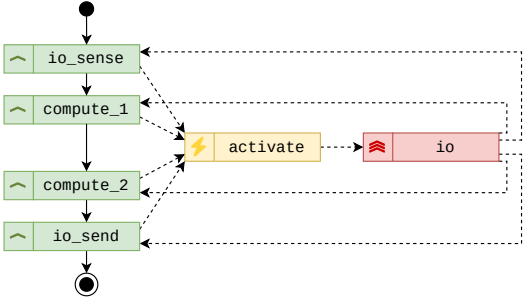
## Application:

```
void taskLow() {
  io_sense();
  compute_1();
  compute_2();
  io_send();
}
```

```
void isr() {
  activate(taskHigh);
}
```

```
void taskHigh() {
  io();
}
```

## Control-Flow Graph:



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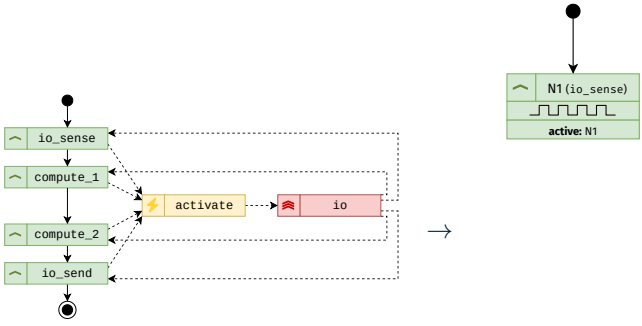
Control-Flow Graph → Power-State–Transition Graph (PSTG):



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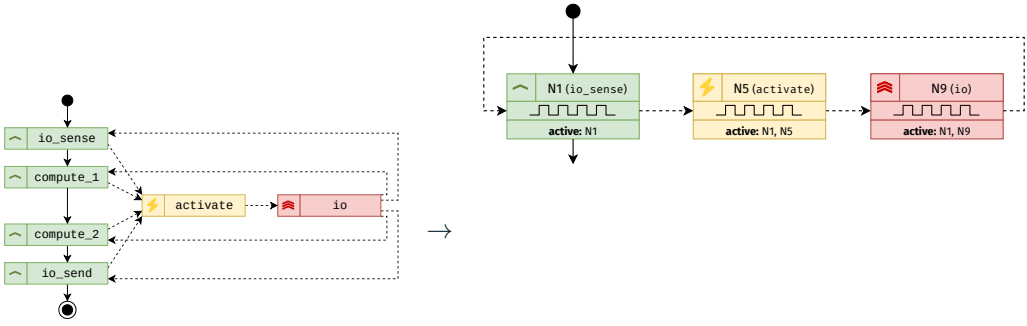

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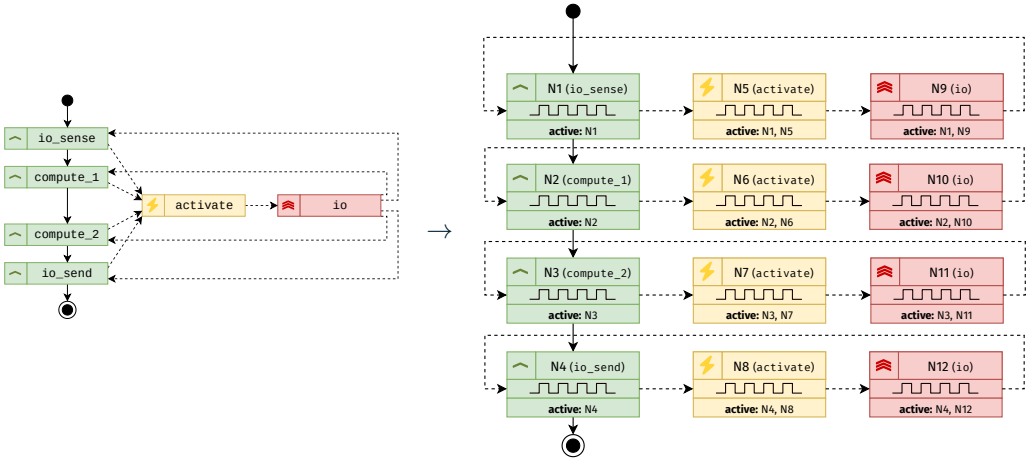

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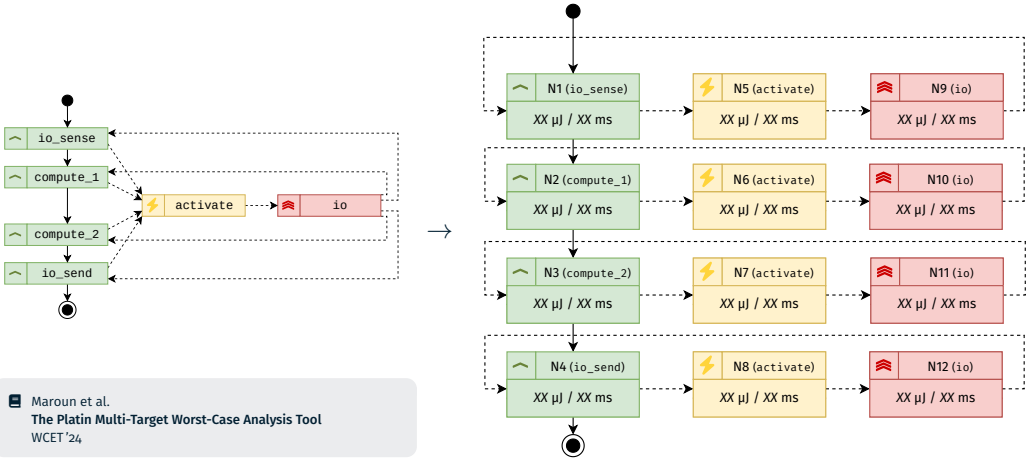
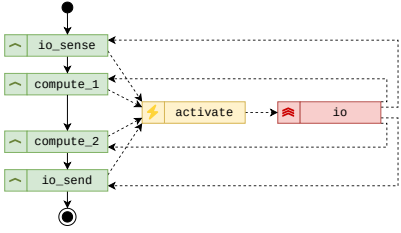


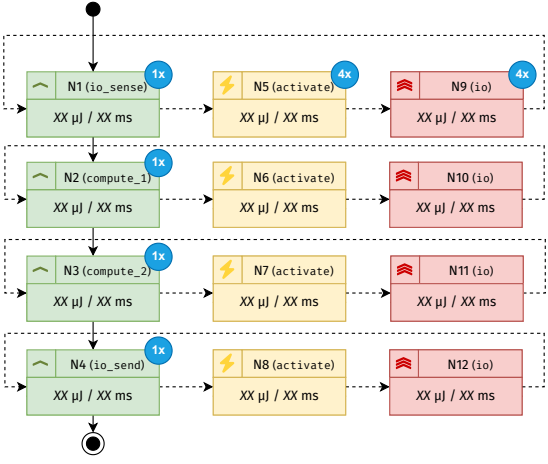

Maroun et al.
**The Platin Multi-Target Worst-Case Analysis Tool**
WCET '24

# The WATWAOS Approach (2)

Control-Flow Graph → Power-State–Transition Graph (PSTG) → ILP




→

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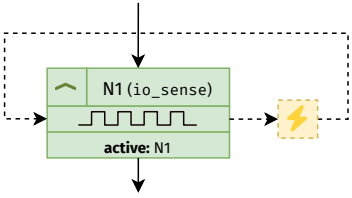
# Integer Linear Program




**Constraints per node:**

- $\sum f(\text{Input Edge}) = \sum f(\text{Output Edge})$
- $f(\text{Node}) = \sum f(\text{Input Edges}_{\neq \text{ISR}})$
- ...

**Other important constraints**

- Loops: derive upper bound from source code
- ISRs: determine frequency using minimum inter-arrival time

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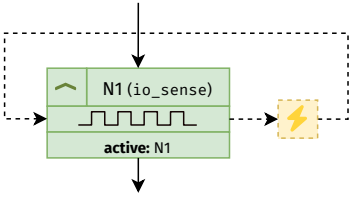


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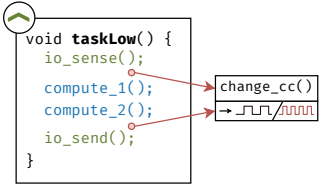
✔ Provide safe WCET/WCEC bounds

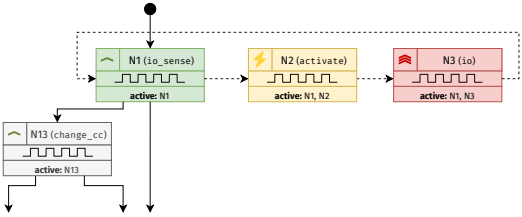
# Adding Clock Reconfiguration Points




**New:** add clock reconfiguration nodes

- before/after single I/O operations
- before/after a loop with I/O operations
- at the start/end of a task

# Adding Reconfiguration Points to the PSTG



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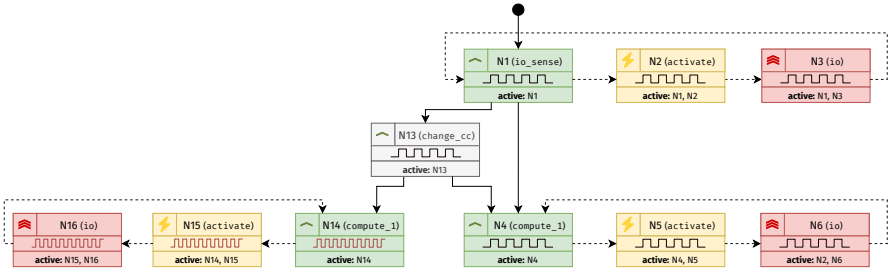

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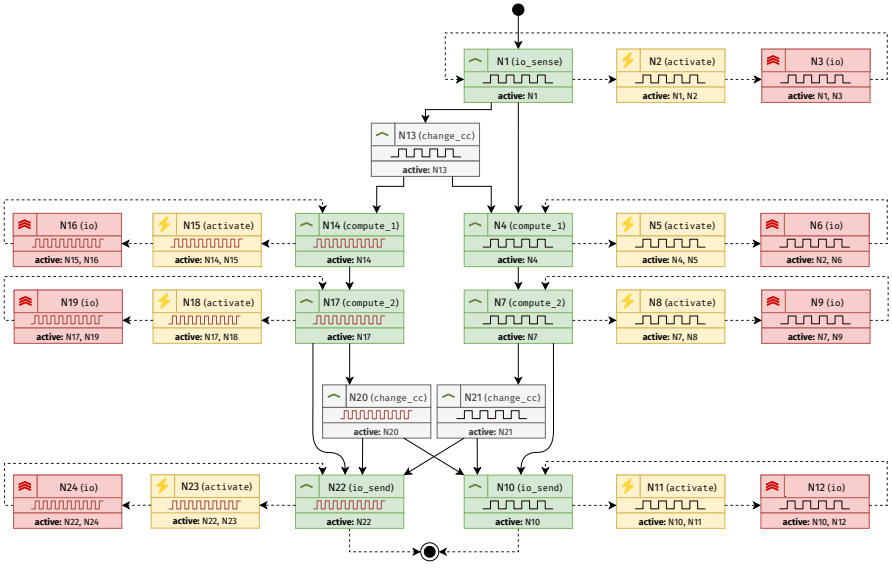

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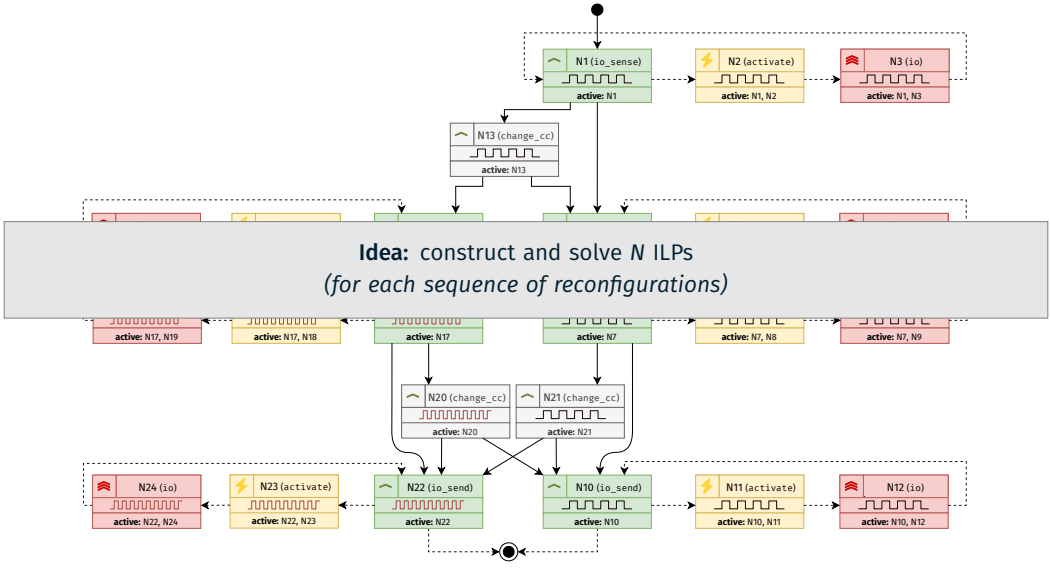


**Idea:** construct and solve *N* ILPs
*(for each sequence of reconfigurations)*

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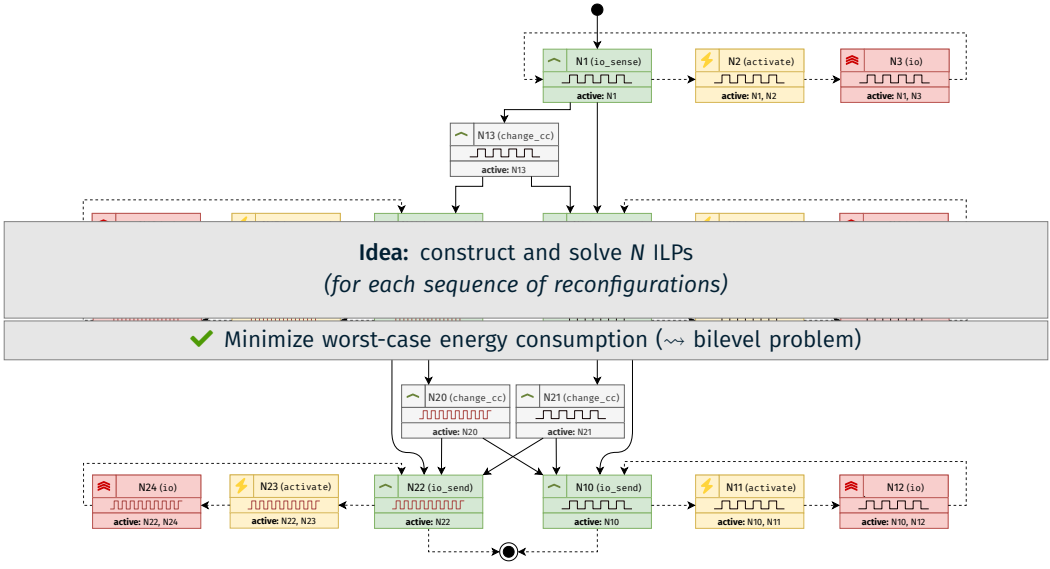

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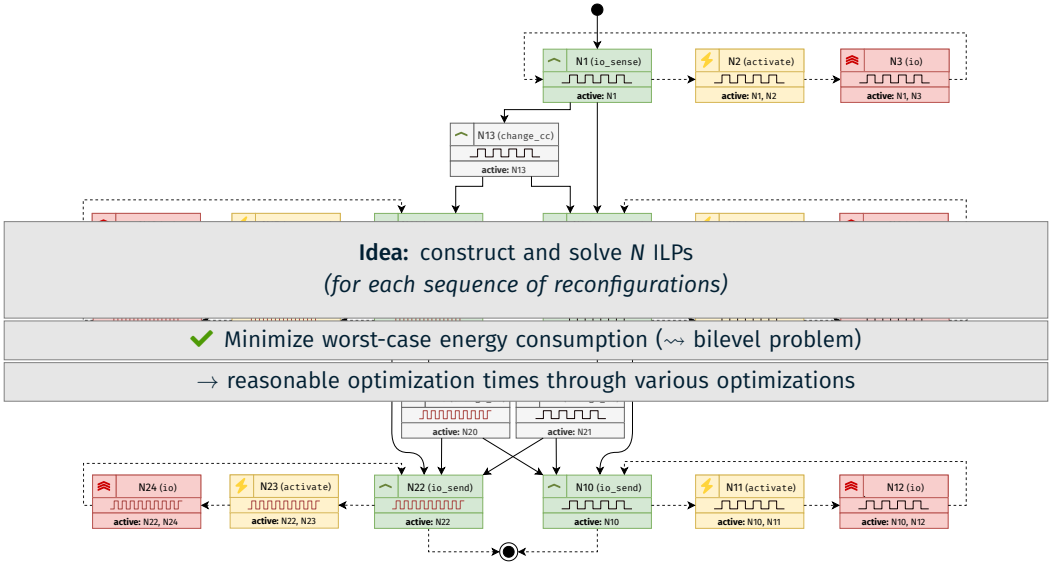


**Idea:** construct and solve *N* ILPs
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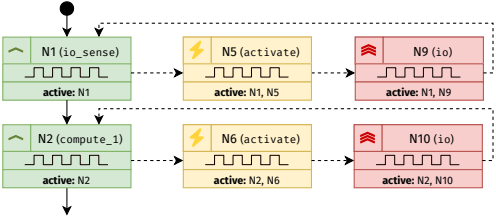
✔ Minimize worst-case energy consumption ($\rightsquigarrow$ bilevel problem)

$\rightarrow$ reasonable optimization times through various optimizations

# Optimization: Exploiting Similarities in the Graph Construction



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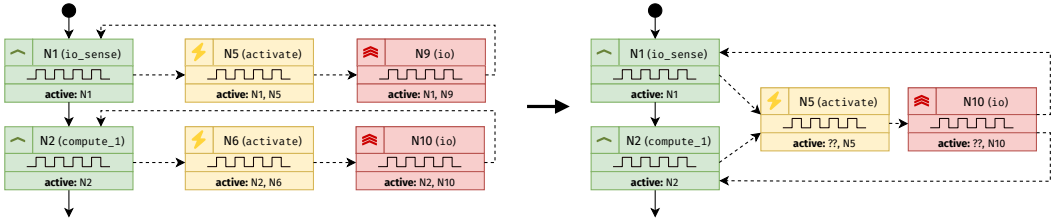
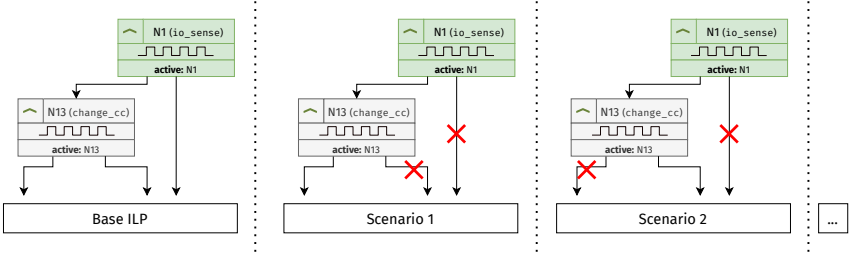



- Idea: merge nodes and edges whenever possible
  - Reduces the amount of constraints and variables in the ILP
  - New constraints necessary to retain context-sensitive information

# Optimization: Exploiting Similarities in the ILP Formulation

- Previously: construct *N* ILPs
- Now: construct 1 base ILP with multiple *scenarios*
  - Feature of the *Gurobi* solver



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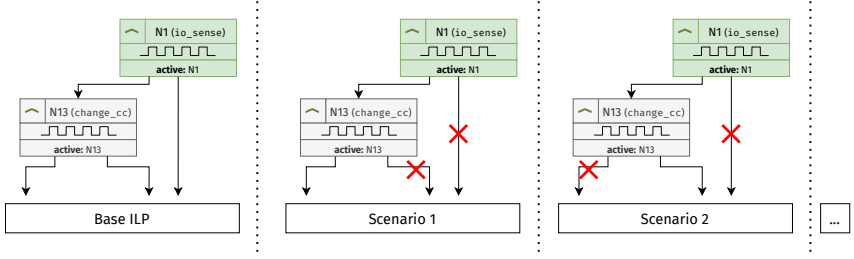
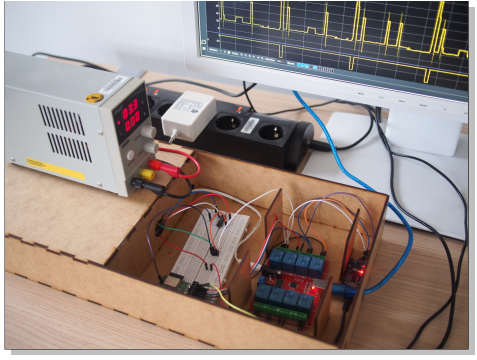


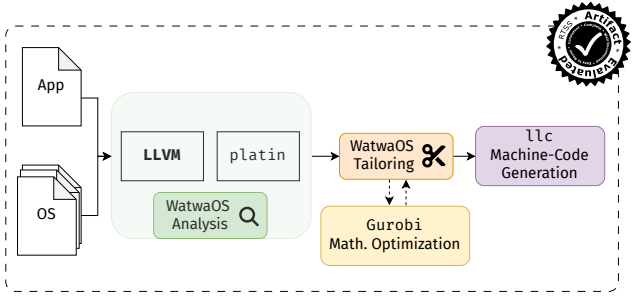

✔ Keep analysis and optimization times reasonable

# Evaluation

# Setup

**ESP32-C3**: 32-bit RISC-V CPU, max. 160 MHz, 400 kB SRAM
**Energy measurement device**: Joulescope JS220





# Evaluation: Optimization Time (1)

| Interrupts | Merging | Variables | Constraints | Solving time *(first 3000 scenarios)* |
|---|---|---|---|---|
| 0 | Off | 98 | 87 | 0.10 s |
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| 1 | Off | 984 | 663 | 2.74 s |
| | On | 270 | 238 | 2.29 s **-16.4 %** |
| 2 | Off | 1854 | 1229 | 9.65 s |
| | On | 430 | 386 | 5.26 s **-45.5 %** |
| 3 | Off | 2724 | 1795 | 13.34 s |
| | On | 590 | 534 | 6.56 s **-50.8 %** |
| 4 | Off | 3594 | 2361 | 15.68 s |
| | On | 750 | 682 | 9.24 s **-41.1 %** |

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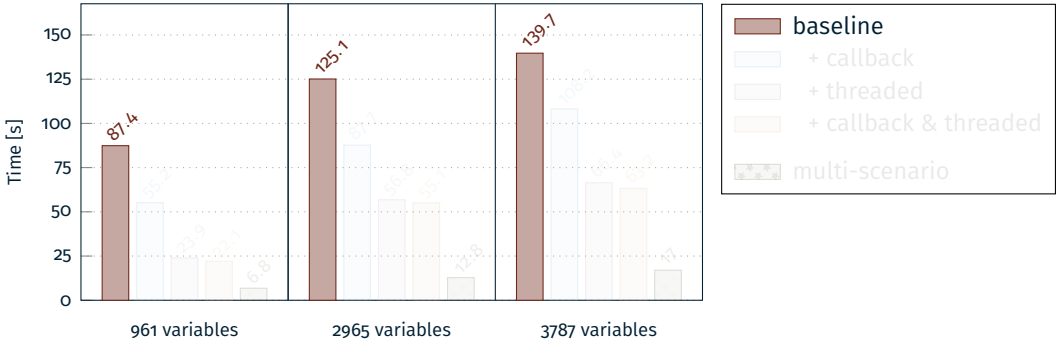
✔ Up to 50 % solving time reduction by exploiting similarities in the PSTG

# Evaluation: Optimization Time (2)



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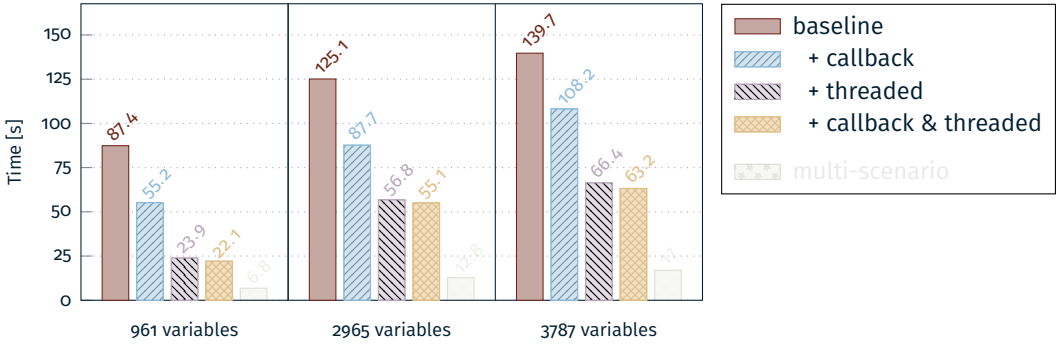

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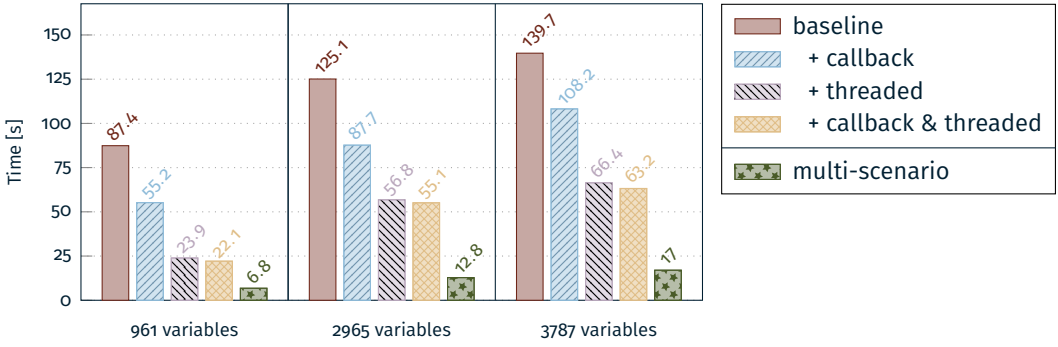
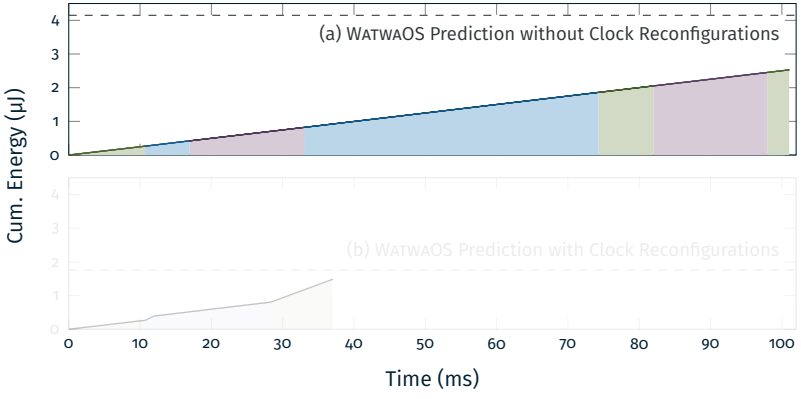



✔ Significant optimization time reduction by optimizing the ILP solving process

# Evaluation: Application Example




| | Predicted | Measured |
|---|---|---|
| **(a)** | 4.15 µJ | 2.52 µJ |

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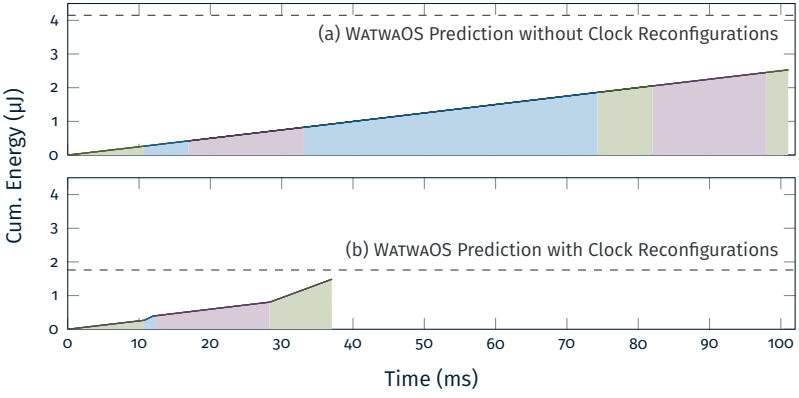


| | Predicted | Measured |
|---|---|---|
| **(a)** | 4.15 µJ | 2.52 µJ |
| **(b)** | 1.76 µJ | 1.48 µJ |

✔ Improved energy efficiency compared to static clock configuration

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WATWAOS Source Code and Artifact: